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circuit and "logic operation" and delay

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1 **Behavioral VHDL transistor slope models**
Dube, J.; Navabi, Z.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International , 23-27 Sep 1991
Page(s): P8 -4/1-4

[Abstract] [PDF Full-Text (372 KB)] **IEEE CNF**

2 **Data flow approach to self-timed logic in VLSI**
Lau, C.H.; Renshaw, D.; Mavor, J.;
Circuits and Systems, 1988., IEEE International Symposium on , 7-9 Jun 1988
Page(s): 479 -482 vol.1

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

3 **Diode-HBT-logic circuits monolithically integrable with ECL/CML circuits**
Wang, K.C.; Beccue, S.M.; Chang, M.F.; Nubling, R.B.; Cappon, A.; Tsen, T.; Chen, D.M.; Asbeck, P.M.; Kwok, C.Y.;
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1991. Technical Digest 1991., 13th Annual , 20-23 Oct 1991
Page(s): 91 -94

[Abstract] [PDF Full-Text (220 KB)] **IEEE CNF**

4 **Static power driven voltage scaling and delay driven buffer sizing in Mixed Swing QuadRail for sub-1 V I/O swings**
Krishnamurthy, R.K.; Lys, I.; Carley, L.R.;

Low Power Electronics and Design, 1996., International Symposium on , 12-14 Aug 1996
Page(s): 381 -386

[Abstract] [PDF Full-Text (572 KB)] **IEEE CNF**

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5 **New TSPC latches and flipflops minimizing delay and power**
Jiren Yuan; Svensson, C.;
VLSI Circuits, 1996. Digest of Technical Papers., 1996 Symposium on , 13-15 Jun 1996
Page(s): 160 -161

[Abstract] [PDF Full-Text (176 KB)] **IEEE CNF**

---

6 **Data-dependent evaluating latched CMOS differential logic family for statistical power reduction**
Bai-Sum Kong; Young-Hyun Jun;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 1 , 2000
Page(s): 760 -763 vol.1

[Abstract] [PDF Full-Text (304 KB)] **IEEE CNF**

---

7 **Energy per logic operation in integrated circuits: definition and determination**
Muller, R.; Pfleiderer, H.-J.; Stein, K.-U.;
Solid-State Circuits, IEEE Journal of , Volume: 11 Issue: 5 , Oct 1976
Page(s): 657 -661

[Abstract] [PDF Full-Text (608 KB)] **IEEE JRN**

---

8 **Low-power SITL IC**
Iwanami, E.; Arai, S.; Shimbo, M.; Tanaka, K.; Watanabe, A.;
Solid-State Circuits, IEEE Journal of , Volume: 17 Issue: 5 , Oct 1982
Page(s): 919 -924

[Abstract] [PDF Full-Text (1000 KB)] **IEEE JRN**

---

9 **Proposal of dual-powered superconducting logic circuits**
Yamada, H.; Tanaka, T.;
Solid-State Circuits, IEEE Journal of , Volume: 20 Issue: 4 , Aug 1985

Page(s): 833 -836

[Abstract] [PDF Full-Text (616 KB)] **IEEE JRN**

10 **Magnetic bubble logic component library**
Jyh-Ping Hwang; Jiin-Chuan Wu; Humphrey, F.;
Magnetics, IEEE Transactions on , Volume: 22 Issue: 4 , Jul 1986
Page(s): 217 -238

[Abstract] [PDF Full-Text (3024 KB)] **IEEE JRN**

11 **Diode-HBT-logic circuits monolithically integrable with ECl/CML circuits**
Wang, K.-C.; Beccue, S.M.; Chang, M.-C.F.; Nubling, R.B.; Cappon, A.M.; Tsen, T.C.-T.; Chen, D.M.; Asbeck, P.M.; Kwok, C.Y.;
Solid-State Circuits, IEEE Journal of , Volume: 27 Issue: 10 , Oct 1992
Page(s): 1372 -1378

[Abstract] [PDF Full-Text (548 KB)] **IEEE JRN**

12 **Race logic architecture (RALA): a novel logic concept using the race scheme of input variables**
Se-Joong Lee; Hoi-Jun Yoo;
Solid-State Circuits, IEEE Journal of , Volume: 37 Issue: 2 , Feb 2002

Page(s): 191 -201

[Abstract] [PDF Full-Text (708 KB)] **IEEE JRN**

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1 Digital CMOS logic operation in the sub-threshold region 80%
Hendrawan Soeleman , Kaushik Roy
Proceedings of the tenth Great Lakes Symposium on VLSI March 2000

Numerous efforts in balancing the trade-off between power, area and performance have been carried out in the medium performance, medium power region of the design spectrum. However, not much study has been done at the two extreme ends of the design spectrum, namely, the ultra-low power with acceptable performance at one end, and high performance with power within limit at the other. In this paper, we focus on the ultra-low power end of the spectrum where performance is of secondary importance ...

2 A hypothetical ALU for use in teaching computer organization 80%
Wayne D. Smith
ACM SIGCSE Bulletin , Proceedings of the sixteenth SIGCSE technical symposium on Computer science education March 1985
Volume 17 Issue 1

3 VHDL: a call for standards 80%
David R. Coelho
Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

With the introduction of the IEEE 1076 version of VHDL, an excellent industry standard hardware description language is now available. VHDL is an extremely flexible and versatile language. As a consequence, the language reference documentation is not sufficient to insure that models written by one hardware designer will be compatible with another's models. What is required is a set of VHDL modelling conventions and standard packages which structure the usage of VHDL modelling approaches. Th ...

4 Static power driven voltage scaling and delay driven buffer sizing in mixed swing QuadRail for sub-1V I/O swings 80%
R. Krishnamurthy , I. Lys , L. Carley
Proceedings of the 1996 international symposium on Low power electronics and design August 1996

5 Electroid-oriented adiabatic switching circuits 80%
David J. Frank , Paul M. Solomon
Proceedings 1995 international symposium on Low power design April 1995

6 Aquarius: Logic simulation on an Engineering Workstation 80%
Andrew Sangster , Jhon Monahan
Proceedings of the twentieth design automation conference on Design automation June 1983

Aquarius is an interactive hierarchical logic simulator designed to run in a multiple window (concurrent processing) environment on an Engineering Workstation. This approach lets an engineer iterate conveniently between simulation and modification of the logic model or input patterns. Because Aquarius is hierarchical, any subtree of the model may be simulated, facilitating bottom-up design verification. Aquarius uses an event-driven selective trace algorithm and 9 logic states. I ...

7 Transmission gate modeling in an existing three-value simulator 77%
Robert M. McDermott
Proceedings of the nineteenth design automation conference January 1982

Existing three value (0, 1, X,) logic simulators cannot support the use of MOS transmission gates, but this deficiency can be easily eliminated by the addition of one logic value - the high impedance (Z) state. This paper demonstrates that complete transmission gate

modeling, including bi-directional operation and Ratio Logic, can be accomplished with this single Z state and explicit node models; and, since four states require the same internal storage as three states, such an enhan ...

8 Design verification of large scientific computers 77%
Howard E. Krohn
Proceedings of the 14th design automation conference January 1977
Large scientific computers containing 2 million gates can be simulated using a combination of block simulation and gate simulation of 450, 000 gates.

9 Test generation systems in Japan 77%
S. Funatsu , N. Wakatsuki , T. Arima
Proceedings of the 12th design automation conference January 1975
With the advent of large scale and medium scale integrated circuit, test and diagnosis of digital logic circuits become more and more difficult to get an efficient and economical goal. In this paper, Test Generation Systems for testing digital logic circuits (IC Cards) in Japan are introduced. One implemented in Nippon Electric Co. is described in detail. Future problems of Test Generation Systems are also briefly discussed.

10 The use of engineering documentation in support of a high density logic test system 77%
Manuel Correia , Richard L. Daubenmire
Proceedings of the fifth annual 1968 design automation workshop on Design automation July 1968
Introduction of System 360 placed unprecedented technical demands on all IBM facilities. This paper describes the application of Engineering Design Automation Information in support of the development and implementation of a manufacturing test data system.

11 Design rule checking and analysis of IC mask designs 77%
B. W. Lindsay , B. T. Preas
The proceedings of the thirteenth design automation conference on Design automation June 1976
An efficient method of producing logical combinations of integrated circuit (IC) masks in numerical form leads to a generalized design rule checking program. The union (OR), intersection (AND) and the complements, as well as topological classification and simple geometric operations, are provided through a set of LOGical MASk Checking (LOGMASC) commands, allowing the designer to construct, for the given IC technology, a tailored set of design rule checks.

These range from simple tolerance c ...

12 A multiple delay simulator for MOS LSI circuits 77%
H. N. Nham , A. K. Bose
Proceedings of the seventeenth design automation conference on Design automation June 1980

This paper describes a multiple delay simulator for MOS LSI circuits. The basic primitives for this simulator are MOS transistor structures where the transistors are evaluated logically. Integer rise and fall delays are associated with each transition and these delays are computed automatically based on device characteristics and circuit capacitances. The simulator has been extensively used for the design verification of production LSI chips.

13 A gate level model for CMOS combinational logic circuits with application to fault detection 77%
Sudhakar M. Reddy , Vishwani D. Agrawal , Sunil K. Jain
21st Proceedings of the Design Automation Conference on Design automation June 1984

A procedure to derive gate level equivalent circuits for CMOS combinational logic circuits is given. The procedure leads to a model containing AND, OR and NOT gates. Specifically it does not require memory elements as does an earlier model and also uses fewer gates. It is shown that tests for classical stuck-at-0 and stuck-at-1 faults in the equivalent circuit can be used to detect line stuck-at, stuck-open and stuck-on faults in the modeled CMOS circuit.

14 Design methodology and microdiagnostics development for a self-checking microprocessor 77%
R. A. Parekhji , N. K. Nanda
ACM SIGMICRO Newsletter , Proceedings of the 22nd annual international workshop on Microprogramming and microarchitecture August 1989
Volume 20 Issue 3

The conventional design of electronic circuits is intolerant to operational faults. Self-checking logic is aimed at online fault detection and can hence be incorporated to achieve reliable operation. In this paper, the design of a self-checking microprocessor is discussed. Self-checking strategies for different functional units are selectively and judiciously applied, and also modified wherever necessary, for the design of the register section, the arithmetic & logic unit and the contro ...

15 CMOS stuck-open fault detection using single test patterns 77%
R. Rajsuman , A. P. Jayasumana , Y. K. Malaiya

Proceedings of the 1989 26th ACM/IEEE conference on Design automation conference June 1989

CMOS combinational circuits exhibit sequential behavior in the presence of open faults, thus making it necessary to use two pattern tests. Two or multi-pattern sequences may fail to detect CMOS stuck-open faults in the presence of glitches. The available methods for augmenting CMOS gates to test CMOS stuck-open faults, are found to be inadequate in the presence of glitches. A new CMOS testable design is presented. The scheme uses two additional MOSFETs, which convert a CMOS gate to either p ...

16 Logic fault simulation on a vector hypercube multiprocessor 77%

F. Ozguner , C. Aykanat , O. Khalid

Proceedings of the third conference on Hypercube concurrent computers and applications - Volume 2 January 1989

Fault simulation is the process of simulating the response of a logic circuit to input patterns in the presence of all possible single faults and is an essential part of test generation for VLSI circuits. Parallelization of the deductive and parallel simulation methods, on a hypercube multiprocessor and vectorization of the parallel simulation method are described. Experimental results are presented.

17 Session 4C: Topics in physical synthesis: Addressing the timing closure problem by integrating logic optimization and placement 77%

Wilsin Gosti , Sunil P. Khatri , Alberto L. Sangiovanni-Vincentelli

Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design November 2000

Timing closure problems occur when timing estimates computed during logic synthesis do not match with timing estimates computed from the layout of the circuit. In such a situation, logic synthesis and layout synthesis are iterated until the estimates match. The number of such iterations is becoming larger as technology scales. Timing closure problems occur mainly due to the difficulty in accurately predicting interconnect delay during logic synthesis.In this paper, we present an algorithm that i ...

18 False-noise analysis using logic implications 77%

A. Glebov , S. Gavrilov , D. Blaauw , V. Zolotov

ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2002

Volume 7 Issue 3

Cross-coupled noise analysis has become a critical concern in today's VLSI designs. Typically, noise analysis makes the assumption that all aggressing nets can simultaneously switch in the same direction. This creates a worst- case noise pulse on the victim net that often leads

to false noise violations. In this article we present a new approach that uses logic implications to identify the maximum set of aggressor nets that can inject noise simultaneously under the logic constraints of the circu ...

19 Poster Session 4: Activity-sensitive clock tree construction for low power 77%

Chunhong Chen , Changjun Kang , Majid Sarrafzadeh
Proceedings of the 2002 international symposium on Low power electronics and design August 2002

This paper presents an activity-sensitive clock tree construction technique for low power design of VLSI clock networks. We introduce the term of node difference based on module activity information, and show its relationship with the power consumption. A binary clock tree is built using the node difference between different modules to optimize the power consumption due to the interconnections (i.e., clock gating signals and clock edges). We also develop a method to determine gating signals with ...

20 Session 8: Automated selective multi-threshold design for ultra-low standby applications 77%

Kimiyoshi Usami , Naoyuki Kawabe , Masayuki Koizumi , Katsuhiro Seta , Toshiyuki Furusawa
Proceedings of the 2002 international symposium on Low power electronics and design August 2002

This paper describes an automated design technique to selectively use multi-threshold CMOS (MTCMOS) in a cell-by-cell fashion. MT cells consisting of low-Vth transistors and high-Vth sleep transistors are assigned to critical paths, while high-Vth cells are assigned to non-critical paths. Compared to the conventional MTCMOS, the gate delay is not affected by the discharge patterns of other gates because there is no virtual ground to be shared. We applied this technique to a test chip of a DSP co ...

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21 Session 3: Closed-loop adaptive voltage scaling controller for standard-cell ASICs 77%

Sandeep Dhar , Dragan Maksimovi? , Bruno Kranzen
Proceedings of the 2002 international symposium on Low power electronics and design August 2002

The paper describes a closed-loop controller for adaptive voltage scaling (AVS) where the supply voltage to a standard-cell ASIC is dynamically adjusted to the minimum value required for the desired system speed. The controller includes a clock generator that provides a low-jitter clock to the ASIC at all steady-state operating points and through transients. To speed up the voltage transient response to step changes in clock frequency, the controller is based on a multiple-tap resettable delay l ...

22 Timing abstraction: An implication-based method to detect multi-cycle paths in large sequential circuits 77%

Hiroyuki Higuchi
Proceedings of the 39th conference on Design automation June 2002

This paper proposes a fast multi-cycle path analysis method for large sequential circuits. It determines whether or not all the paths between every flip-flop pair are multi-cycle paths. The proposed method is based on ATPG techniques, especially on implication techniques, to utilize circuit structure and multi-cycle path condition directly. The method also checks whether or not the multi-cycle path

may be invalidated by static hazards in combinational logic parts. Experimental results show that ...

23 PALMINI—fast Boolean minimizer for personal computers 77%

L. B. Nguyen , M. A. Perkowdki , N. B. Goldstein
24th ACM/IEEE conference proceedings on Design automation conference October 1987

This paper describes a fast and efficient method for minimization of two level single output Boolean functions. The minimization problem is reduced to that of coloring of the graph of incompatibility of implicants. The program permits also to remove static hazards and allows inversion of output's polarity which proves to be very convenient when designing with PAL's. It gives solutions within a very reasonable amount of time. On small industrial examples its speed is slightly better than Esp ...

24 An automated design of minimum-area IC power/ground nets 77%

S. Chowdhury
24th ACM/IEEE conference proceedings on Design automation conference October 1987

Given tree topologies for routing power/ground (p/g) nets in integrated circuits, this paper formulates and solves the problem of determining the widths of the branches of the trees. Constraints are developed in order to maintain proper logic levels and switching speed, to prevent electromigration, and to satisfy certain design rule and regularity requirements. The area required by the p/g distribution system is minimized subject to these constraints. Some case studies are also presented.

25 A vector hardware accelerator with circuit simulation emphasis 77%

A. Vladimirescu , D. Weiss , M. Katevenis , Z. Bronstein , A. Kifir , K. Danuwidjaja , K. C. Ng. , N. Jain , S. Lass
24th ACM/IEEE conference proceedings on Design automation conference October 1987

A floating-point vector accelerator has been built which runs circuit simulation efficiently. The design considerations of the accelerator are based on the time-consuming parts of SPICE2, available off-the-shelf parts, advanced software tools experience and cost/performance. The three board accelerator can run the entire application program compiled from a high-level language. A personal workstation, such as the PC-AT, is used for the general I/O tasks such as file handling and n ...

26 Low-power design of sequential circuits using a quasi-synchronous 77%

derived clock

Xunwei Wu , Jian Wei , Massoud Pedram , Qing Wu
Proceedings on the 2000 conference on Asia and South Pacific design automation January 2000

27 A large scale cellular array processor: AAP-1 77%
Toshio Kondo , Tayoshi Nakashima , Toshio Tsuchiya , Yoshi Sugiyama , Tsuneta Sudo
Proceedings of the 1985 ACM thirteenth annual conference on Computer Science March 1985

A SIMD cellular array processor called the Adaptive Array Processor (AAP-1) has been developed. Its 256 x 256 array of bit-organized processing elements (PEs) is composed of 1024 custom nMOS LSIs and occupies the small volume of 0.33m3. Extensive parallelism offers ultra-high throughout for various types of two-dimensional data processing, together with data-dependent operation capability through the use of control registers in each PE. The processing speed has experime ...

28 An analytical method for finding the maximum crosstalk in lossless-coupled transmission lines 77%
Ali El-Zein , Salim Chowdhury
Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design November 1992

29 Architecture of a massively parallel processor 77%
Kenneth E. Batcher
25 years of the international symposia on Computer architecture (selected papers) August 1998

30 Algorithm for vectorizing logic simulation and evaluation of “VELVET” performance 77%
Yoshiharu Kazama , Yoshiaki Kinoshita , Motonobu Nagafuji , Hiroshi Murayama
Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

A very large-scale logic simulation engine “VELVET” has been developed. VELVET is a vectorized event-driven simulator which can handle simultaneously both gate-level logic and Register Transfer Level structure. VELVET can process simulation jobs two orders of magnitude faster than a conventional gate-level simulator. This paper describes how to realize such high performance, an algorithm for vectorizing the simulation and performance.

31 Reduced instruction set computers 77%

David A. Patterson
Communications of the ACM January 1985
Volume 28 Issue 1

Reduced instruction set computers aim for both simplicity in hardware and synergy between architectures and compilers. Optimizing compilers are used to compile programming languages down to instructions that are as unencumbered as microinstructions in a large virtual address space, and to make the instruction cycle time as fast as possible.

32 Synthesis of instruction sets for pipelined microprocessors 77%

Ing-Jer Huang , Alvin M. Despain
Proceedings of the 31st annual conference on Design automation conference June 1994

33 A polynomial-time heuristic approach to approximate a solution to the false path problem 77%

Shiang-Tang Huang , Tai Ming Parng , Jyuo Min Shyu
Proceedings of the 30th international on Design automation conference July 1993